EP0745868

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Temperature compensated APD detector bias and transimpedance amplifier circuitry for laser range finders

Abstract:

Abstract of EP0745868<br 12f5 > Laser range finder circuitry (FIG. 1) including an avalanche photodiode detector (315), a capacitor (C1) for storing a detector bias voltage, and a transimpedance amplifier (317) for amplifying the detector signal. The capacitor (C1) is charged in response to a first control signal (IUP) by a circuit employing first and second field effect transistors (Qb1, Qb2) and is discharged in response to a second control signal (IDN) by a circuit employing a third field effect transistor (Qb4). An overload protection circuit including a single diode (CR3) is provided to accommodate excessive charge created by backscatter upon initial laser firing. A temperature sensor (319) is provided to develop a temperature signal which may be monitored to adjust the detector bias voltage and other parameters so as to permit use of an associated laser range finder over a wide range of temperatures.

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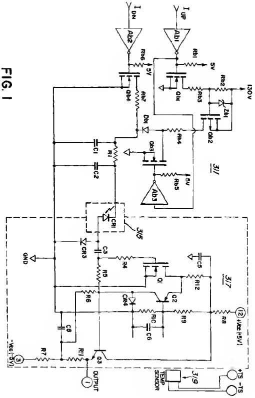
(54) Temperature compensated APD detector bias and transimpedance amplifier circuitry for laser range finders

(57) Laser range finder circuitry (FIG. 1) including an avalanche photodiode detector (315), a capacitor (C1) for storing a detector bias voltage, and a transimpedance amplifier (317) for amplifying the detector signal. The capacitor (C1) is charged in response to a first control signal (I_{UP}) by a circuit employing first and second field effect transistors (Q_{b1}, Q_{b2}) and is discharged in response to a second control signal (I_{DN}) by a circuit employing a third field effect transistor (Q_{b4}). An overload protection circuit including a single diode (CR3) is provided to accommodate excessive charge created by backscatter upon initial laser firing. A temperature sensor (319) is provided to develop a temperature signal which may be monitored to adjust the detector bias voltage and other parameters so as to permit use of an associated laser range finder over a wide range of temperatures.

FIG. 1



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Description

BACKGROUND OF THE INVENTION

1. Field of the Invention

The subject invention relates to laser range finder circuitry and, more particularly, to improved detector bias and transimpedance amplifier circuitry particularly useful with APD laser range finder receivers.

2. Description of Related Art

Present laser range finder receivers rely on photodiodes for detection of target returns. There are two major categories of receiver photodiodes for detection: the acceptor intrinsic donor ("PIN") diode, and the avalanche photodiode ("APD"). Either type of device can be based on indium gallium arsenide ("InGaAs") or germanium technology. The PIN diode is the most commonly used, but requires a signal of 60 nanowatts to 100 nanowatts for a 99% probability of detection. Uncooled APD receivers currently in use are capable of 99% detection with a signal of about 10 nanowatts. Because the greater sensitivity of the APD detectors translates into a greater maximum system range, they are preferred for fabrication of a universal device applicable to a family of eye-safe laser range finders.

Current APD receivers rely on a bias network that instantaneously steps the bias voltage down by some number of volts. This instantaneous step causes the transimpedance amplifier ("TIA"), which amplifies the detector signal, to saturate. The recovery from this effect can take as long as a microsecond. The saturation condition is due to current flowing through the parasitic capacitor across the detector (approximately 1 pF) during the step voltage transition. Under these conditions a diode must be used in the TIA circuit in order to clamp the input of the TIA. This diode adds parasitic capacitance on the order of 0.8 pF, which reduces circuit sensitivity and significantly increases the cost of the detector/preamplifier (TIA).

Present APD receivers are optimized at room temperature and, therefore, are significantly suboptimal at other operating temperatures. System sensitivity over temperature thus cannot be guaranteed. A number of components are also required for testing the frequency response of present APD amplifiers.

OBJECTS AND SUMMARY OF THE INVENTION

It is therefore an object of the invention to improve laser systems;

It is another object to improve laser range finder circuitry;

It is another object of the invention to improve detector bias and transimpedance amplifier circuitry applicable to laser range finders;

It is another object to increase sensitivity of laser range finder systems; and

It is another object to significantly improve sensitivity of laser range finder systems over temperature ranges such as -40 to +85°C while decreasing cost.

According to the APD biasing concept of the invention, simple current sources are used to charge and discharge the APD bias voltage. The discharge rate is slow enough that an insignificant amount of current flows through the parasitic capacitance across the APD. The transimpedance amplifier or TIA remains within its small signal dynamic range, allowing for very fast settling after the charging current source is disabled. Additionally, the clamp diode can be eliminated, resulting in a significant improvement in the sensitivity of the system. The number of components within the detector/ preamplifier package can also be reduced.

According to another aspect of the invention, the addition of an on-substrate temperature sensor allows the system to operate at peak sensitivity over all operating conditions. According to another aspect of the invention. the frequency response of the system is measured by illuminating the APD detector with an unmodulated CW source and examining the noise spectrum at the output of the TIA. The noise spectrum will have a power envelope versus frequency that is characteristic of the detector/preamplifier (TIA) frequency response. Additional parasitic capacitance and all of the components required to test frequency response in the prior art are eliminated. Thus, the net effect of the invention is lower cost and significantly higher yield due to increased margin on sensitivity, as well as optimal system performance over operating temperature extremes.

BRIEF DESCRIPTION OF THE DRAWING

The objects and features of the present invention, which are believed to be novel, are set forth with particularity in the appended claims. The present invention, both as to its organization and manner of operation, together with further objects and advantages, may best be understood by reference to the following description, taken in connection with the accompanying drawing.

FIG. 1 is an electrical circuit diagram of an APD bias circuit and transimpedance amplifier according to the preferred embodiment.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The following description is provided to enable any person skilled in the art to make and use the invention and sets forth the best modes contemplated by the inventors of carrying out their invention. Various modifications, however, will remain readily apparent to those skilled in the art, since the generic principles of the present invention have been defined herein specifically

to provide circuitry optimized for performance and ease of manufacture.

As shown in FIG. 1, the preferred embodiment of the invention includes an APD bias circuit 311, an APD detector 315, and a transimpedance amplifier circuit 317. While the detector 315 is preferably an APD device, other detector devices, such as PINs, can be used in various embodiments according to the invention.

With respect to the APD bias circuit 311, I_{UP} and I_{DN} signals are applied to the inputs of respective inverter amplifiers A_{b1}, A_{b2}, for example, by a system microcontroller (not shown). The output of the inverter A_{b1} is applied to the gate of a first bias circuit field effect transistor (FET) Q_{b1} and to the input of a second inverter amplifier A_{b3}. The gate of the first bias circuit FET Q_{b1} is connected through a resistor R_{b1} to a reference voltage (+5 volts). The source of the first FET Q_{b1} is connected to ground, while its drain is connected to a first terminal of a resistor R_{b3}. The second terminal of the resistor R_{b3} is connected to a first terminal of a resistor R_{b2} and to the gate of a second bias circuit FET Q_{b2}. The second terminal of the resistor R_{b2} and the source of the second bias circuit FET Q_{b2} are connected in common to a 130-volt dc supply voltage. A zener diode Z_{b1} is connected in parallel with the resistor R_{b2}.

The drain of the second bias circuit FET Q_{b2} is connected to a first terminal of a resistor R_{b4} whose second terminal is connected to the anode of a diode D_{b1} and to the drain of a third bias circuit FET Q_{b3}. The source of the third bias circuit FET Q_{b3} is connected to ground, while its gate is connected to one terminal of a resistor R_{b5} and to the output of the inverter amplifier A_{b3}. The second terminal of the resistor R_{b5} is connected to a 5-volt dc reference voltage.

The cathode of the diode D_{b1} is connected to a first terminal of a bias voltage storage capacitor C1 and to the drain of a fourth bias circuit FET Q_{b4}. whose source is grounded. The gate of the fourth bias circuit FET Q_{b4} is connected to the output of the inverter amplifier A_{b2} and to one terminal of a resistor R_{b6} whose second terminal is connected to the 5-volt dc reference voltage.

The bias voltage storage capacitor C1 has its first terminal further connected to one terminal of a resistor R1 whose second terminal is connected to a shunt capacitor C2 and to the cathode of the APD detector diode CR1. The second terminal of the capacitor C2 is grounded. The anode of the APD diode CR1 is connected to the anode of a PN diode CR3 whose cathode is further connected to ground. An AC coupling capacitor C3 connects the anode of the APD detector diode CR1 to the input of the transimpedance amplifier 317.

The input to the transimpedance amplifier 317 comprises a node constituting the intersection of the first terminals of respective resistors R4 and R5. The second terminal of the resistor R4 is connected to the gate of a first FET Q1, whose source is connected to ground and whose drain is connected to the first terminal of a resistor R12 and the emitter of an NPN transistor Q2. The second terminal of the resistor R12 is connected to one terminal of a capacitor C5 whose opposite terminal is grounded, as well as to the collector of a PNP transistor Q3.

The collector of the second transistor Q2 is connected to the anode of a PN diode CR4 and to the junction point of the second terminal of the resistor R5 and the first terminal of a resistor R6. The cathode of the PN diode CR4 is connected to one terminal of a capacitor C6 whose second terminal is connected to the base of the transistor Q2. The base of the transistor Q2 is further connected via a resistor R9 to the second terminal of the resistor R12 and to a resistor R8 whose second terminal is connected to the 5-volt dc reference voltage.

The base of the third transistor Q3 is connected to the second terminal of the resistor R5, which thus constitutes a feedback resistor from the output to the input of the amplifier 317. The emitter of the third transistor Q3 constitutes the output of the transimpedance amplifier circuit 317 and is further connected to the first terminal of a resistor R11. The second terminal of the resistor R11 is connected to the first terminal of a resistor R7, whose second terminal is connected to a -5-volt dc reference voltage. The first terminal of the resistor R7 is further connected to a first terminal of a capacitor C8 and to the second terminal of the resistor R6. The second terminal of the capacitor C8 is grounded. Examples of typical components for circuitry constructed according to the preferred embodiment are as follows:

TABLE

Resistances K(Ω)	Other Components
R_{b1} - 2	C1 - 22 nF
R_{b2} - 4.7	C2 - 10 pF
R_{b3} - 100	C3 - 15 pF
R_{b4} - 200	C5 - .01 μF
R_{b5} - 2	C6 - 10 nF
R_{b6} - 2	C8 - .01 μF
R_{b7} - 200	CR3 - HP 5082
R1 - 3.3	CR4 - HP 5082
R4 - .02	Q1 - NEC71000MVC
R5 - 51	Q2 - 2N4957
R6 - 1	Q3 - 2N2857
R7 - .01	
R8 - .01	
R9 - 1.27	
R10 - 1	
R11 - 2.3	
R12 - .160	

The foregoing values are illustrative only and may be varied in various embodiments for optimal performance in various laser range finder systems.

In operation of the circuit of FIG. 1, I_{UP} and I_{DN} control signals are selectively applied, for example, by a mi-

crocontroller. The control signal I_{UP} turns on FET Q_{b2} by turning off FET Q_{b1}, causing the gate of the FET Q_{b2} to float up in voltage. The increase in voltage permits current to flow from the 130-volt source through the resistor R_{b4} and the diode D_{b1}, causing the voltage on the bias voltage storage capacitor C1 to increase until such time as the I_{UP} control signal is turned off. The open collector type of logic gate is particularly designed to drive FETs such as FET Q_{b1}.

When the I_{UP} control signal is off, the FET Q_{b3} turns on, shorting the resistor R_{b4} to ground so as to drain off leakage current from FET Q_{b2} in order to prevent such current from further charging the capacitor C1. While I_{UP} is off, the diode D_{b1} serves to maintain the bias voltage held by the capacitor C1; i.e., it prevents discharge of the capacitor voltage by current flow through the FET Q_{b3}. The bias voltage held by the capacitor C1 may range from 30 volts to 90 volts and is determined by the length of time I_{UP} is "on" and the breakdown voltage of the APD 315.

Application of the I_{DN} control signal turns on the FET Q_{b4} and discharges the bias voltage storage capacitor C1 to ground through the resistor R_{b7}. Both I_{UP} and I_{DN} are off when the circuitry is inactive.

Once the bias voltage storage capacitor C1 has been charged, the detector circuit 315 is biased for operation, for example, to detect a laser pulse return after firing of a laser. When the laser is initially fired, a large amount of energy is reflected or "back-scattered" back into the laser range finder optics, causing the TIA amplifier 317 to saturate. Accordingly, the diode CR3 is employed in the circuit to become forward biased by the increase in detector voltage and to dump the charge to ground; i.e., the diode CR3 comprises protection circuitry for accommodating initial overloads. The circuit provided by the capacitor C2 and the resistor R1 connected to the APD 315 limits the amount of energy which can be dumped through the diode CR3. After the diode CR3 stops conducting, the voltage on the capacitor C2 rapidly increases, via charging current flow through the capacitor C1 and the resistor R1.

The capacitor C3 is an AC coupling capacitor, which connects the detector circuit to the TIA 317. The TIA 317 itself may be viewed as a typical operational amplifier having a feedback resistor R5 connected between its output and inverting input which, in an illustrative embodiment, has a value of 51 KΩ.

In the preferred TIA amplifier 317 shown in FIG. 1, the current flowing into the R4-R5-C3 node is multiplied by the value of the feedback resistor R5, producing an output voltage at the emitter of the third transistor Q3. The FET Q1 has a "gm" parameter associated with it, which is basically a voltage-to-current converting factor. As current flows through the coupling capacitor C3, the gate voltage on the FET Q1 rises, causing more current flow through the FET Q1. The transistor Q2 tries to hold the drain of the FET Q1 at a constant voltage. Thus, as the FET Q1 "asks" for more current, the transistor Q2 turns off. As the transistor Q2 shuts off, in order to hold steady state, its collector voltage moves down, producing a voltage across the feedback resistor R5. For the selected value of R5 of 51 KΩ, this voltage ultimately equals 51 KΩ times the current flowing through the AC coupling capacitor C3. The transistor Q3 is a buffer-follower whose emitter voltage side is .7 below the voltage on its base (i.e., the voltage developed across the feedback resistor R5).

The TIA amplifier resistor R6 can be used to achieve a manufacturing advantage according to the preferred embodiment. The stability of the amplifier is a function of the open loop gain, which is determined by the "gm" of the FET Q1 and the value of the resistor R6. Thus, if gm changes, the value of R6 may be adjusted to compensate for it. Thus, in production, an entire wafer of FETs Q1 may be fabricated. After R6 is adjusted to get proper compensation for one of the FETs Q1 from the wafer, all devices on that wafer can be used with the same R6 value.

As to the remainder of the components, resistors R9 and R10 bias the transistor Q2 and set its operating point. The capacitor C6 makes the node an AC short circuit. The diode CR4 prevents circuit overload. The resistors R7 and R11 are respectively used for power supply isolation and to bias the second transistor Q3.

The feedback resistor R5 determines the amount of transimpedance gain, i.e., current-to-voltage transfer. Whatever current goes through C3 x 51K equals the output voltage swing. The feedback resistor R5 further determines the ultimate bandwidth of the system. Lowering the value of R5 provides more bandwidth, enabling the system to operate with shorter laser pulses.

The detector 315 and TIA amplifier 317 are preferably formed as a hybrid circuit on a common substrate such as alumina. A temperature sensor 319 is mounted on the substrate next to the detector 315 and enables optimizing the receiver as a function of temperature. Thus, an associated microcontroller may continuously monitor and recalibrate the receiver as a function of temperature. The temperature sensor 319 may be a commercially available AD590 sensor wherein a reference voltage is applied to a first terminal +TS, producing a current at a second terminal -TS which is related to temperature. This current is converted to a voltage which enables an associated microcontroller to read the temperature of the detector 315.

The frequency response of the system of FIG. 1 is measured by illuminating the detector 315 with an unmodulated CW source and looking at the noise spectrum at the output TIA OUT of the amplifier 317. The noise spectrum will have a power envelope versus frequency that is characteristic of the detector/preamplifier frequency response. The frequency response of the amplifier will vary from part to part due to the "gm" parameter of the preferred NEC71000 GaAs FET. The feedback loop can compensate for this effect by adjusting the values of the resistors R5 and R6. This is an impor-

tant cost savings because the select-in-test only occurs once for each lot-buy of the NEC71000 FET. Therefore, the value of the resistor R6 is selected on the first unit and is fixed for the balance of the production run. The value of the resistor R5 is not normally changed because it affects the amount of output voltage.

Another feature of this design is the addition of the temperature sensor 319 within the detector/preamplifier package. The optimum detector bias voltage can shift dramatically with temperature changes. The temperature sensor 319 allows the system to monitor this condition and self-calibrate the receiver operating parameters, such as receiver offset voltages, false alarm rate, and APD bias voltage. Essentially, the receiver can be optimized for performance over the entire operating temperature range.

The receiver sensitivity is optimized by increasing the APD bias voltage (this increases the APD gain) until the APD noise is larger than the electronics noise. Once the APD noise begins to dominate the electronics noise of the preamplifier 317, further increases in APD gain will reduce the system NEP (noise equivalent power). At low temperatures, the APD gain must be high in order to overcome the preamplifier noise. This is due to low leakage currents within the APD at low temperatures. Under these conditions, the APD noise may not be larger than the preamplifier noise because of limitations in achievable APD gain. All of these effects can be optimized by monitoring the APD temperature along with self-calibrating electronics.

Those skilled in the art will appreciate that various adaptations and modifications of the just-described preferred embodiment can be configured without departing from the scope and spirit of the invention. Therefore, it is to be understood that, within the scope of the appended claims, the invention may be practiced other than as specifically described herein.

Claims

1. Laser range finder apparatus comprising:

    a photodiode detector (315) having a first terminal and a second output terminal;
    a charge storage device (C1) connected to the first terminal of said photodiode detector (315) for storing a detector bias voltage;
    a current source (R_{b1}, Q_{b1}, R_{b3}, R_{b2}, Z_{b1}, Q_{b2}, R_{b4}) connected to said charge storage device (C1) and responsive to a first control signal to apply a charging current to said charge storage device (C1); and
    a circuit including a transistor switch (Q_{b4}) connected to said charge storage device and responsive to a second control signal to discharge said charge storage device (C1).

2. The laser range finder apparatus of Claim 1 further including a trans impedance amplifier (317) having an input connected to said second output terminal and an output.

3. The laser range finder apparatus of Claim 1 wherein said current source (R_{b1}, Q_{b1}, R_{b3}, R_{b2}, Z_{b1}, Q_{b2}, R_{b4}) includes a first field effect transistor (Q_{b2}) having a first terminal connected to a voltage source, said field effect transistor (Q_{b2}) being switchable to cause supply of said charging current to said charge storage device (C1).

4. The laser range finder apparatus of Claim 3 wherein said current source (R_{b1}, Q_{b1}, R_{b3}, R_{b2}, Z_{b1}, Q_{b2}, R_{b4}) includes a second field effect transistor having a gate terminal connected to receive said first control signal and a first terminal connected through a resistance (R_{b3}) to the gate of said first field effect transistor (Q_{b2}).

5. The laser range finder apparatus of Claim 4 further including a third field effect transistor (Q_{b3}) having a gate, an inverter (A_{b3}) having an output connected to said gate, said inverter having an input connected to receive said first control signal, said third field effect transistor (Q_{b3}) further having a first terminal connected to the anode of a diode (D_{b1}) and a second terminal connected to ground, said diode (D_{b1}) further having a cathode connected to said charge storage device (C1).

6. The laser range finder apparatus of Claim 1 further including an overload protection circuit including a diode (CR3) connected to said photodiode detector (CR1) and to ground.

7. The laser range finder apparatus of Claim 1 wherein said overload protection circuit further includes a resistor-capacitor network (R1, C2) having a connection to said photodiode detector (CR1) for limiting the amount of excess charge which can be dumped through said diode (CR3).

8. The laser range finder apparatus of Claim 2 wherein said transimpedance amplifier (317) applies a current-to-voltage transfer factor to a current at its input so as to produce a voltage at its output which is a multiple of said current.

9. The laser range finder apparatus of Claim 8 wherein said transimpedance amplifier (317) includes a field effect transistor (Q1) and a first resistance (R6) and has an open loop gain determined by a parameter "gm" of said field effect transistor (Q1) and by the value of said first resistance (R6); and wherein the value of said first resistance (R6) is adjusted to compensate for variations in the parameter "gm" in or-

der to maintain a desired open loop gain.

10. The laser range finder apparatus of Claim 8 wherein said transimpedance amplifier 317 further includes a feedback resistance (R5) whose value is said multiple.

11. The laser range finder apparatus of Claim 8 wherein said feedback resistance (R5) is adjustable to increase the bandwidth of said apparatus.

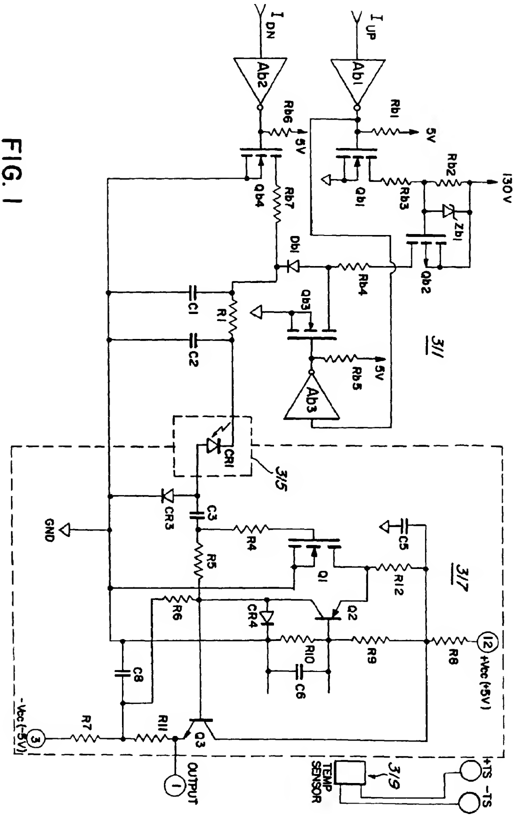
12. The laser range finder apparatus of Claim 1 wherein said photodiode detector (CR1) comprises an avalanche photodiode.

13. The apparatus of Claim 1 further including a temperature sensing circuit (319) mounted in the vicinity of said photodiode detector (CR1) for monitoring the temperature in said vicinity and providing a signal indicative thereof.

14. A method of measuring the frequency response of a system employing a photodiode detector (CR1) whose output is amplified by a transimpedance amplifier (317) comprising the steps of:

    illuminating the detector (CR1) with an unmodulated continuous wave (cw) source; and
    examining the noise spectrum at the output of the transimpedance amplifier (TIA-317).

15. The method of Claim 14 wherein the power envelope versus frequency of the noise spectrum is characteristic of the photodetector/ TIA frequency response.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Ab2
Ab3
Rb1
Rb2
Rb3
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Rb5
Rb6
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5V
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Qb3
Qb4
Zb1
Db1
C1
C2
C3
C5
C6
C8
R1
R4
R5
R6
R7
R8
R9
R10
R11
R12
CR1
CR3
CR4
Q1
Q2
Q3
3/1
3/5
3/7
3/9
GND
12
+Vcc (+5V)
3
-Vcc (-5V)
1
OUTPUT
TEMP SENSOR
+TS
-TS

FIG. 1

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 96 30 3505

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	US-A-4 415 803 (MUOI) * abstract; figure 1 * ---	1	G01S7/486
A	US-A-4 882 482 (SMITH ET AL) * the whole document * -----		
			TECHNICAL FIELDS SEARCHED (Int.Cl.6)
			G01S H03F H04B H03G

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
BERLIN	6 August 1996	Danielidis, S

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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